

REMARKS

The application is believed to be in condition for allowance.

Applicants note that the IDS filed on July 31, 2003 (copy of the PTO-1449 enclosed) has not been initialed and returned. An initialed copy is requested.

Independent claims 1 and 19 have been amended to make explicit the feature of the invention that avoids two sub-pixels of a pixel from having both a minimum gradation level and a maximum gradation level. That is, a first sub-pixel represents a minimum gradation level, the other sub-pixels are restricted from representing the maximum gradation level. Likewise, when the first sub-pixel represents a maximum gradation level, the other sub-pixels are restricted from representing the minimum gradation level.

Applicants note with appreciation that the Official Action indicated that claims 4-11 and 14 were directed to allowable subject matter.

Claims 1-3, 12-13, and 18-22 stand rejected as anticipated by HIRAKAWA et al. 6,097,358; and claims 15-17 as obvious over HIRAKAWA et al.

Claims 1 and 19 are not anticipated as HIRAKAWA et al. do not disclose the recited feature that "when a first sub-pixel of said plurality of sub-pixels represents one of a minimum

gradation level and a maximum gradation level of said plurality of gradation levels, a second sub-pixel of said plurality of sub-pixels adjacent to said first sub-pixel is always restricted to represent other than the other of said minimum gradation level and said maximum gradation level so that when a first sub-pixel of the pixel represents a minimum gradation level, the other sub-pixels of the pixel are restricted from representing the maximum gradation level and when the first sub-pixel represents a maximum gradation level, the other sub-pixels are restricted from representing the minimum gradation level".

For this feature, the Official Action has offered Figures 1-6, column 6, lines 22-67 and column 11, lines 1-36.

None of these disclose the above-noted recitation of claims 1 and 19.

FIG. 1 is a diagram illustrating the structure of a plasma display 100 according to the present invention.

The drawing figures show a plasma display layout (Figure 1), a set of sub-pixels (Figure 2), and schematic views of the disclosed driving methods.

The passage from column 6 discloses the general operation of the plasma display 100 of Figure 1, including selectively lighting a large number of cells C composing a screen SC.

There is disclosed a three-electrode surface discharge PDP in which pairs of sustain electrodes X and Y are disposed in parallel as the first and second main electrodes and define cells as display elements at their intersections with address electrodes A as the third electrodes. There is also disclosed that the drive unit 80 includes a controller 81, a frame memory 82, a data processing circuit 83, a sub-field memory 84, a power source circuit 85, an X driver circuit 87, a Y driver circuit 88 and an address driver circuit 89. Field data DF is representative of luminance levels of the individual cells, i.e., gradation levels.

However, applicants do not see that there is any disclosure of restricting the luminance level as recited, so that when a first sub-pixel of a pixel represents a minimum gradation level, the other sub-pixels of the pixel are restricted from representing the maximum gradation level and when the first sub-pixel represents a maximum gradation level, the other sub-pixels are restricted from representing the minimum gradation level.

The relied-upon passage from column 11 is reproduced below:

"Since the entire screen is thus charged by two steps by use of the remaining wall charge, more uniform charge distribution can be obtained compared with the case where a

charged state is formed only by one discharge. Thus the reliability of the addressing is improved.

"FIG. 6 is a schematic view illustrating a modified driving method in accordance with the present invention.

"In a specific sub-field group (SFG3 in the example shown in the figure), a cell whose wall charge is erased in one address period is subjected to the erase addressing in at least one address period(s) TA after that address period by use of the same sub-field data DSF. Thus, even if there is a failure in the address discharge and a cell which should not emit light happens to emit light, the unnecessary wall charge in the cell is erased by repeating the erase addressing and the cell falls in the non-light-emitting state. In usual cases, the first erase addressing rarely fails to erase the unnecessary wall charge. Accordingly, a discharge hardly takes place in the second and later erase addressing and the contrast of display does not decline.

"The above-described repeated addressing can be performed in all the sub-field groups SFG1 to SFG3. However, taking it into consideration that a failure in the address discharge rarely happens and, if it happens, it affects little a sub-field having a small luminance weight (luminance rises only slightly by erroneous emission of light), it is desirable that the specific sub-field group be selected in descending order of luminance weight or the sum of luminance weights in the sub-field

groups. For, in the case where the address discharge successfully takes place in the first addressing and the discharge does not take place in the second and later addressing, the application of the scan pulse P_y and the address pulse P_a consumes power for charging the cell. It may also be effective for reducing power consumption to limit the number of repeated addressings to one, two or three."

Although there is disclosure concerning luminance level control, applicants do not believe that the recited feature of the invention is disclosed. Since there is no disclosure of restricting the luminance level so that when a first sub-pixel of a pixel represents a minimum gradation level, the other sub-pixels of the pixel are restricted from representing the maximum gradation level and when the first sub-pixel represents a maximum gradation level, the other sub-pixels are restricted from representing the minimum gradation level, the anticipation rejection is not viable.

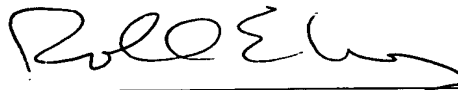
Reconsideration and allowance of all the pending claims are respectfully requested.

Applicants believe that the present application is in condition and an early indication of the same is respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17.

Respectfully submitted,

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REL/lrs

APPENDIX:

The Appendix includes the following item:

- copy of Form PTO-1449 filed July 31, 2003

(Use several sheets if necessary)

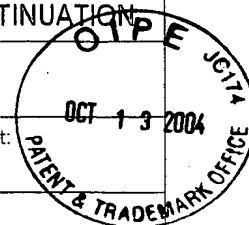
8022-1058

NEW CONTINUATION

Daigo SASAKI et al.

July 31, 2003

Group Art Unit:

[illegible]

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
	3-2722	1/9/1991	JAPAN			*	
	11-143437	5/28/1999	JAPAN			*	
	0 471 275	2/19/1992	EUROPE			*	
	2-168231	6/28/1990	JAPAN			*	
	0 880 125	11/25/1998	EUROPE			*	
	10-68931	3/10/1998	JAPAN				
	2576765	11/7/1996	JAPAN				
	2000-206922	7/28/2000	JAPAN				
	11-231827	8/27/1999	JAPAN				

		Atsushi TOGAMI et al., Estimation of Shape Effect on Area Intensity Method with DT-CNN, pages 391-398, The Institute of Electronics Information and Communication Engineers

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

* Abstract provided for the Examiner's convenience

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